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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,106	06/20/2005	Ian D French	GB02 0245 US	1444

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EXAMINER	
TYNAN, MATTHEW	
ART UNIT	**PAPER NUMBER**
2871	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,106	FRENCH ET AL.	
	Examiner	Art Unit	
	Matthew Tynan	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al. (U.S. Patent No. 5,541,748).

4. Regarding claim 1, Ono et al. teaches a method of forming an active plate for an LCD comprising:

- Depositing and patterning a substantially transparent conductor layer (ITO1 (d1), Fig. 1) to define an array of pixel electrodes over an insulating substrate arranged in rows and columns (see Fig. 1).
- Defining row conductors (GL, Fig. 1) and connected gate conductor portions (see Fig. 1) over different areas of the insulating substrate to the pixel electrodes (Fig. 1).
- Depositing and patterning thin film transistor layers (GI, AS) over the gate conductor portions to form transistor bodies, the thin film transistor layers comprising at least a gate insulator (GI) and a semiconductor layer (AS).

- Forming an insulating layer (AS, GI, Fig. 1) arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes of two adjacent columns (see Fig. 1; also, claims 2-3) of pixels;
- Forming an opaque conductor layer (d2) over the substrate and patterning the opaque conductor layer to define column conductors (DL, d2, d3) on top of the insulating layer, and source (SD1) and drain (SD2) electrodes for the transistor on top of the thin film transistor layers, one of which is connected to a column conductor and the other of which is connected to an associated pixel electrode.

5. Regarding claim 2, Ono et al. teaches the thin film transistor layers (GI, AS) also overlap an adjacent pixel electrode (see Fig. 1, Fig. 3).

6. Regarding claim 9, Ono et al. teaches a liquid crystal display device comprising an active plate and a passive plate with liquid crystal sandwiched between, wherein the active plate comprises:

- An insulating substrate (e.g. SUB1, Fig. 2)
- An array of rows and columns of pixel electrodes (ITO1; Fig. 2).
- An array of row conductors (GL), occupying different areas over the over the substrate.
- The pixel electrodes being substantially transparent (inherent, made of ITO).
- The row conductors having gate conductor portions (see Fig. 1).
- Thin film transistor layers (GI, AS) over the gate conductor portions to define transistor bodies,

- An insulating layer (GI, AS) arranged as a plurality of columns, each insulating layer column overlapping the pixel electrodes of two adjacent columns of pixels.
- Opaque column conductors (d2) provided on top of the insulating layer;
- Source and drain electrodes (SD1, SD2) for the transistor on top of the thin film transistor layers one of which is connected to a column conductor and the other of which is connected to an associated pixel electrode.

7. Regarding claim 10, Ono et al. teaches the thin film transistor layers define, in addition to the transistor bodies, columns which lie beneath the insulating layer (see col. 8, lines 46-51).

Claim Rejections - 35 USC § 103

8. Claims 3-4 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,541,748) in view of den Boer et al. (U.S. Patent No. 6,307,215, referred to as "Boer" hereinafter).

9. Ono et al. has been discussed above regarding claims 1 and 9.

10. Regarding claims 3 and 11, Ono et al. does not teach the insulating layer comprises a polymer.

11. However, Boer teaches (col. 6, lines 37-59) the insulating layer (33) between an overlapped pixel electrode and a data line should be made from a polymer material with a low dielectric constant in order to reduce capacitive cross-talk (col. 6, lines 54-64).

12. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method and device taught by Ono et al. using the insulating layer taught

by Boer in order to reduce capacitive cross-talk between the overlapped pixel electrode and data line.

13. Regarding claims 4 and 12, Boer teaches a the polymer is a photo-acrylic polymer (col. 6, lines 60-64) with a suitably low dielectric constant to reduce capacitive cross-talk.

14. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,541,748) in view of Tsutsui et al. (U.S. Patent No. 5,032,531).

15. Ono et al. has been discussed above regarding claim 1. Regarding claim 5, Ono et al. does not teach that defining the pixel electrodes and the row conductors is performed with a first, single-mask process.

16. However, Tsutsui et al. teaches using a single photoresist mask in order to simultaneously pattern a gate electrode, pixel electrode, and a scanning line (i.e. row conductor), thereby reducing the number of required photoresist masks.

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method taught by Ono et al. using the single mask process taught by Tsutsui et al. in order to reduce the number of required photoresist masks.

18. Regarding claim 6, Ono et al. teaches forming the transistor bodies and the insulating layer with a single-mask process (col. 19, "Process E").

19. Regarding claim 7, Ono et al. teaches forming the column conductors and the source and drain electrodes using a third, single-mask process (col. 19-20, "Process F").

20. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (U.S. Patent No. 5,541,748) and Tsutsui et al. (U.S. Patent No. 5,032,531) as applied to claim 7 above, and further in view of Kim et al. (U.S. Pub. No. 2002/0021403).

21. The combination of Ono et al. and Tsutsui et al. does not teach using a half-tone mask.

22. However, Kim et al. teaches that the advantage of using a half-tone mask is that it allows simultaneous patterning of stacked layers by a single etching step ([0062], lines 1-2), thus reducing the number of processing steps.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method taught Ono et al. and Tsutsui et al. using the halftone mask as taught by Kim et al. in order to reduce the number of processing steps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Tynan whose telephone number is 571-270-1433. The examiner can normally be reached on Mon-Fri. 7:30-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-4491. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MT

ANDREW SCHECHTER
PRIMARY EXAMINER